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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kelkar et al.

Attorney Docket No.: NSC1P284/P05753

Patent: 7,095,116 B1

Issued: August 22, 2006

Title: ALUMINUM-FREE UNDER BUMP METALLIZATION STRUCTURE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on February 2, 2007 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Aurelia M. Sanchez

REQUEST FOR CERTIFICATE OF CORRECTION OF OFFICE MISTAKE (35 U.S.C. §254, 37 CFR §1.322)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where the errors are shown correctly in the application file are as follows:

CLAIMS:

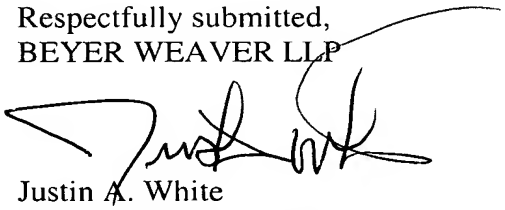
1. In line 19 of claim 7 (column 10, line 33) change "ton to bottom" to --top to bottom--. This appears correctly in the Response to Final Office Action as filed on May 18, 2006, on page 3, paragraph 4, line 12, as claim 8.

2. In line 1 of claim 14 (column 11, line 7) change "where said" to --wherein said--. This appears correctly in the Response to Final Office Action as filed on May 18, 2006, on page 5, paragraph 4, line 1, as claim 23.

Patentee hereby requests expedited issuance of the Certificate of Correction because the error lies with the Office and because the error is clearly disclosed in the records of the Office. As required for expedited issuance, enclosed is documentation that unequivocally supports the patentee's assertion without needing reference to the patent file wrapper.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NSC1P284).

Respectfully submitted,
BEYER WEAVER LLP



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(Also Form PT-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,095,116 B1 Page 1 of 1

DATED : August 22, 2006

INVENTOR(S) : Kelkar et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Claims:

In line 19 of claim 7 (column 10, line 33) change "ton to bottom" to --top to bottom--.

In line 1 of claim 14 (column 11, line 7) change "where said" to --wherein said--.

MAILING ADDRESS OF SENDER:

PATENT NO. 7,095,116 B1

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3. (Original) The semiconductor wafer of claim 1, wherein one or more of said plurality of under bump metallization stacks has a total thickness of less than about 15 kilo-angstroms.

4. (Original) The semiconductor wafer of claim 3, wherein one or more of said plurality of under bump metallization stacks has a total thickness of less than about 12 kilo-angstroms.

5. (Canceled)

6. (Currently Amended) The semiconductor wafer of claim **1** ~~5~~, wherein said passivation layer comprises a compound selected from the group consisting of silicon dioxide and silicon nitride.

7. (Canceled)

8. (Currently Amended) An integrated circuit device, comprising:

a plurality of contact pads formed on a first surface of said device;

a passivation layer disposed on said first surface, said passivation layer including a plurality of passivation layer vias formed therethrough and associated with at least a portion of said plurality of contact pads;

a resilient layer defining a substantially horizontal plane and disposed on said passivation layer, said resilient layer having a plurality of resilient layer vias formed therethrough and associated with at least a portion of said plurality of contact pads and at least a portion of said plurality of passivation layer vias, wherein one or more of said plurality of resilient layer vias

defines a primary axis extending therethrough and perpendicular to said substantially horizontal plane, and

contains one or more sidewalls that are **fully tapered from top to bottom such that no portion of sidewall is** ~~not~~ substantially parallel to said primary axis; and

a plurality of solder bumps, wherein one or more of said plurality of solder bumps are each coupled with an associated under bump metallization stack and an associated contact pad.

16-20 (Canceled)

21. (Previously Presented) The integrated circuit device of claim 8, wherein said resilient layer completely covers all top and side surfaces of said passivation layer at at least a portion of said plurality of passivation layer vias.

22. (Previously Presented) The integrated circuit device of claim 8, wherein said passivation layer comprises a silicon based material.

23. (Previously Presented) The integrated circuit device of claim 22, wherein said passivation layer comprises one or more materials selected from the group consisting of SiO_2 and SiN.

24. (Previously Presented) The integrated circuit device of claim 8, wherein said resilient layer comprises benzocyclobutene or a polyimide.

25. (Currently Amended) An integrated circuit device, comprising:

a plurality of contact pads formed on an active surface of said device;

an inorganic passivation layer disposed upon said active surface, said passivation layer including a plurality of passivation layer vias formed therethrough and associated with at least a portion of said plurality of contact pads;

a polymeric resilient layer defining a substantially horizontal plane and disposed upon and substantially covering said passivation layer, said resilient layer having a plurality of resilient layer vias formed therethrough and associated with at least a portion of said plurality of